TE. SEM VII (CBSGS) - ETRX

C.O.

May 2015

Q.P. Code : **5049**

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt **any three** questions out of **remaining five** questions.
(3) Assume suitable data **wherever** necessary.
(4) Figures to the right indicate **full marks**.

1 (a) Write microinstructions for executing instruction Add Ro, [R3] in three bus architecture processor. **5**

(b) Write a note on nanoprogramming. **5**

(c) Differentiate SRAM and DRAM. **5**

(d) What is parallel processing? **5**

2. (a) Draw flowchart for non-restoring division. Solve (8) ÷ (3) using non-restoring division method. **10**

(b) Differentiate between Horizontal and vertical micro architecture. **10**

3. (a) Consider main memory size is three pages. Following page address trace is generated by execution of a program **10**

2 3 2 1 5 2 4 5 3 2

Assume main memory is cleared initially. Find page hit ratio by

(i) FIFO (ii) LRU replacement scheme.

(b) What is microprogramming? Draw and explain microprogrammed control unit. **10**

4. (a) What is virtual memory? How paging is useful in implementing virtual memory? **10**

(b) State the advancements in arithmetic and logical instructions supported by IA-32 architecture. Describe five floating point arithmetic instructions in IA-32. **10**

5. (a) Explain various DMA transfer modes in brief with examples. **10**

(b) Explain various types of hazards in pipelined processors with example. Also propose solution for each type. **10**

6. (a) What are different I/O access methods? Explain in detail. **10**

(b) Write short notes on :- **5**

(i) Cache coherency **5**

(ii) RISC and CISC architectures.

JP-Con. 10227-15.